temperature such as thermal interfaces on both the top and bottom of the housing. Increased surface area combined with airflow around those surfaces increases the heat removal rate. The housing design could also enable easy interface with an external heat sink. While thermal conduction and infrared radiation techniques are the common methods, application of alternate cooling methods are possible. For example, thermionic emission as described in commonly-assigned U.S. patent application Ser. No. 10/408,471, entitled "Power Circuitry With A Thermionic Cooling System," by Reno Rossetti, which is hereby incorporated by reference, is one method of heat removal that can be used to cool down power devices.

Integration of other logic circuitry including power delivery and control functions in a single package presents additional challenges. For one, the housing requires more pins to interface with other electronic functions. The package should allow for both high current power interconnects in the package and low current signal interconnections. Various packaging technologies that can address these challenges include chip-to-chip wire bonding to eliminate special interface pads, chip-on-chip to save space inside the housing, and multi-chip modules that allow distinctive silicon technologies to be incorporated into a single electronic function. Various embodiments for multi-chip package techniques are described in commonly-assigned U.S. patent application Ser. No. 09/730,932, entitled "Stacked Package Using Flip Chip in Leaded Molded Package Technology," by Rajeev Joshi, and U.S. Pat. No. 10/330,741, entitled "Multichip Module Including Substrate with an Array of Interconnect Structures," also by Rajeev Joshi, both of which are hereby incorporated by reference in their entirety.

While the above provides a complete description of the preferred embodiments of the invention, many alternatives, modifications, and equivalents are possible. For example, many of the charge balancing techniques are described herein in the context of a MOSFET and in particular a trench gated MOSFET. Those skilled in the art will appreciate that the same techniques can apply to other types of devices, including IGBTs, thyristors, diodes and planar MOSFETs, as well as lateral devices. For this and other reasons, therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a drift region of a first conductivity type;

a well region extending above the drift region and having a second conductivity type opposite the first conductivity type;

an active trench extending through the well region and into the drift region, the active trench having its sidewalls and bottom lined with dielectric material, and substantially filled with a first conductive layer and a second conductive layer, the second conductive layer forming a gate electrode and being disposed above the first conductive layer and separated therefrom by inter-electrode dielectric material;

source regions having the first conductivity type formed in the well region adjacent the active trench; and

a charge control trench extending deeper into the drift region than the active trench and substantially filled with material to allow for vertical charge control in the drift region.

2. The semiconductor device of claim **1** wherein a source electrode electrically couples a conductive material inside the charge control trench to the source region.

3. The semiconductor device of claim **1** wherein inside the charge control trench is disposed a plurality of conductive layers stacked vertically and separated from each other and from the trench sidewalls by dielectric material.

4. The semiconductor device of claim **3** wherein the plurality of conductive layers inside the charge control trench are electrically biased to provide vertical charge balancing in the drift region.

5. The semiconductor device of claim **4** wherein the plurality of conductive layers inside the charge control trench are configured to be independently biased.

6. The semiconductor device of claim **3** wherein thicknesses of the plurality of conductive layers inside the charge control trench vary.

7. The semiconductor device of claim **1** wherein the thickness of a first conductive layer that is deeper inside the charge control trench is smaller than the thickness of a second conductive layer that is disposed above the first conductive layer.

8. The semiconductor device of claim **1** wherein the first conductive layer inside the active trench forms a first shield electrode configured to be electrically biased to a desired potential.

9. The semiconductor device of claim **1** wherein the first shield electrode and the source regions are configured to be electrically coupled to substantially the same potential.

10. The semiconductor device of claim **4** wherein the plurality of conductive layers inside the charge control trench are configured to be tied together electrically.

11. The semiconductor device of claim **4** wherein at least one of the plurality of conductive layers is within the drift region.

12. The semiconductor device of claim **4** wherein all of the plurality of conductive layers are within the drift region.

13. The semiconductor device of claim **4** wherein at least one of the plurality of conductive layers is outside of the drift region.

14. The semiconductor device of claim **4** wherein at least one of the plurality of conductive layers is within the p+ heavy body regions.

15. The semiconductor device of claim **4** wherein at least one of the plurality of conductive layers is within the body region.

16. The semiconductor device of claim **4** wherein one of the plurality of conductive layers is located within both the body region and the drift region.

17. The semiconductor device of claim **1** further comprising a second charge control trench located next to the active control trench on the opposite side of the charge control trench wherein the second charge control trench extends deeper into the drift region than the active trench and substantially filled with material to allow for vertical charge control in the drift region.

18. The semiconductor device of claim **17** wherein the charge control trench and the second charge control trench are positioned substantially the same distance away from the active control trench.

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